

Quasi-Delay-Insensitive Computing Device: Methodological and Algorithmic Aspects

Abstract

The approaches to self-timed hardware design are presented. The conditions of intersystem integration of synchronous and self-timed devices are considered through the example of the quasi-delay-insensitive computing device development. This device performs functions of division and square root extraction. It operates with numbers of single and double precisions corresponding to the IEEE 754 standard.