Self-timed Circuits for Low Power and Highly Reliable Microprocessors

S.G. Bobkov[1], M.S. Gorbunov[1], Yu.G. Diachenko[2], Yu.V. Rogdestvenski[2], Yu.A. Stepchenkov[2], A.V. Surkov[1]

[1]Department of Russian Academy of Sciences Institute of System Researches,

bobkov@cs.niisi.ras.ru, gorbunov@cs.niisi.ras.ru, surkov@cs.niisi.ras.ru

[2]Department of Russian Academy of Sciences Institute of Informatics Problems,

{YDiachenko, YRogdest, YStepchenkov}@ipiran.ru

EXTENDED ABSTRACT

Keywords – microprocessors, KOMDIV, self-timed circuits, supercomputers.

The purpose of this article is to provide an introduction to self-timed (ST) circuits design, the results of practical experiment with hybrid Globally Synchronous Locally Asynchronous circuit design, and some conclusions on the consumption reduction and increased robustness of high performance microprocessor, as a result of using self-timed unit.

The double precision divider unit which is a part of FPU of our microprocessor KOMDIV-64 was chosen for the experiment. Two divider units were designed for comparative analysis: one is pure synchronous divider, and another is a self-timed one using speculative indication. Both units have the same functionality. The main goal of the experiment was to achieve the lower power consumption at the same data rate, if possible. As a result, the power consumption of ST divider reveals about 60% reduction of consumption against the synchronous one. But a productivity of ST divider drops as twice as low in compare to synchronous divider. Also we made an experiment with a power supply variations of ST divider unit. It becomes possible because of special design of the chip – the area with a asynchronous part was made in a fully isolated power domain with its own asynchronous testing environment. The asynchronous testing environment may provide the autonomous cycling tests, which results are available for the observation on the special out pin of the chip. As a result of the experiment, the stable work of ST divider in +/-40% power supply variation range is proven.

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