SELF-TIMED CIRCUITRY RETROSPECTIVE

Victor Zakharov, Yury Stepchenkov,
Yury Diachenko, Yury Rogdestvenski

Federal Research Center
“Computer Science and Control”
of Russian Academy of Sciences

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- Self-timed circuit features
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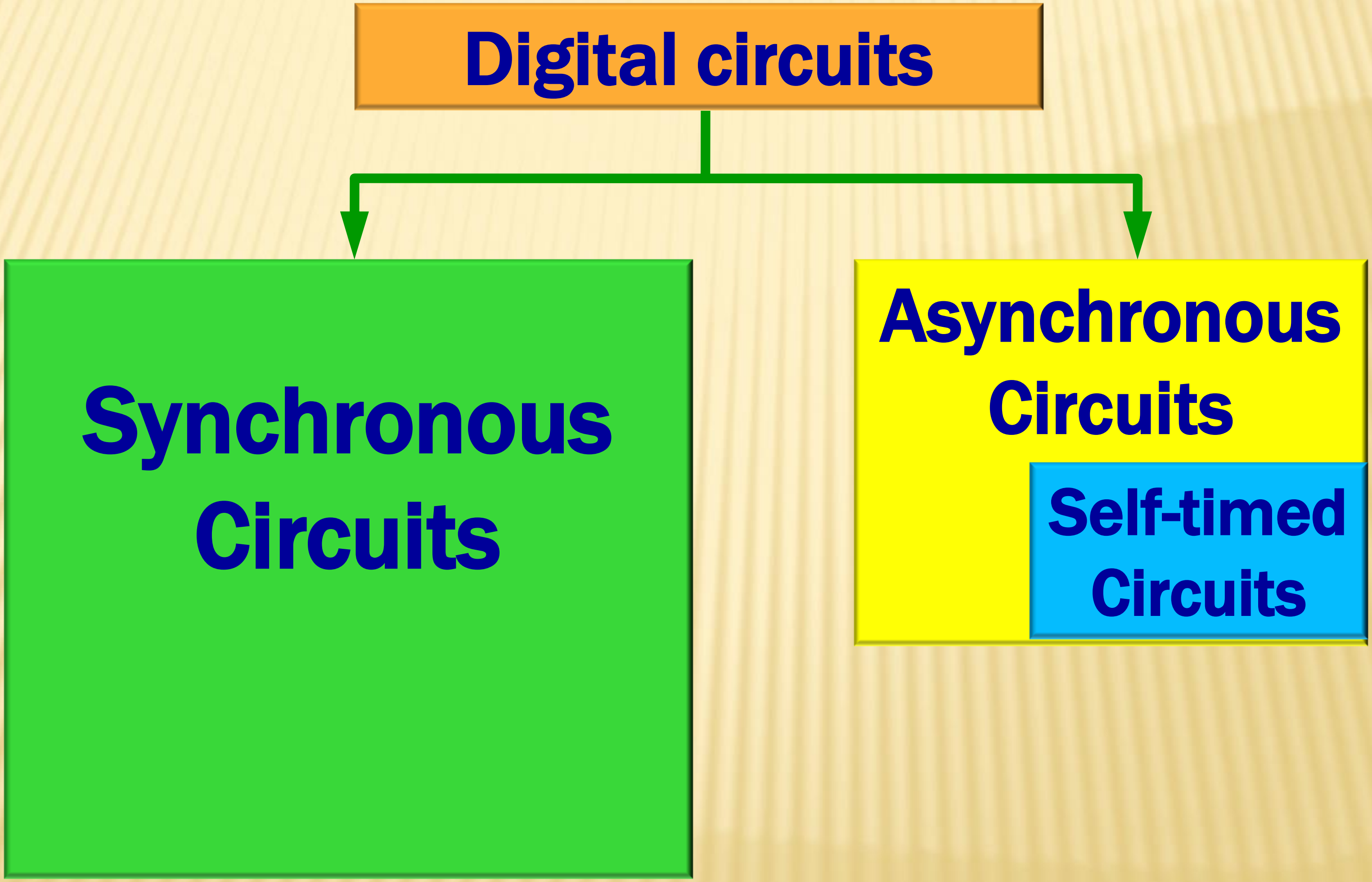
CIRCUITS DESIGN METHODOLOGIES



SELF-TIMED CIRCUIT FEATURES

- **Advantages:**
  - **Stable operation under any operating conditions**
  - **Wide range of workability**
  - **Natural full self-checking concerning constant faults**
  - **Lack of overhead hardware and energy costs associated with global clock tree**
- **Drawbacks:**
  - **Hardware redundancy**
  - **Increased number of signals**

SELF-TIMED CIRCUIT TYPES

Quasi-Speed-Independent (QSI) circuits

- ❖ Do not depend on cell’s delays
- ❖ Critical path indication only

Speed-Independent (SI) circuits

- ❖ Do not depend on cell’s delays
- ❖ Full indication
- ❖ Purely self-timed in isochronous zone

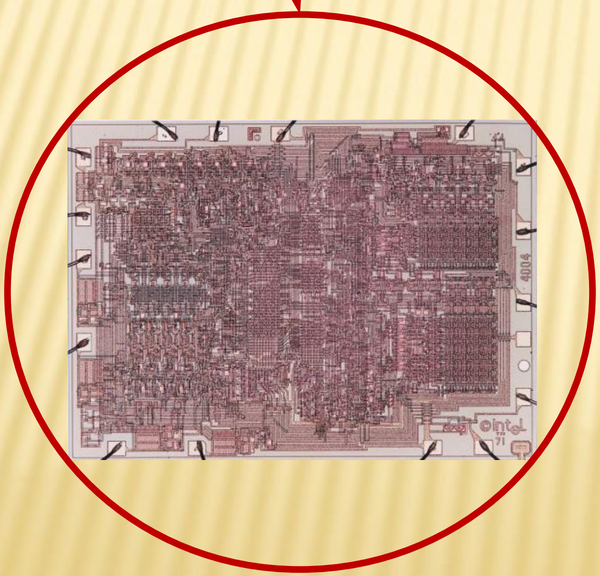
Delay-Insensitive (DI) circuits

- ❖ Do not depend on delays both in cells and wires
- ❖ Full indication

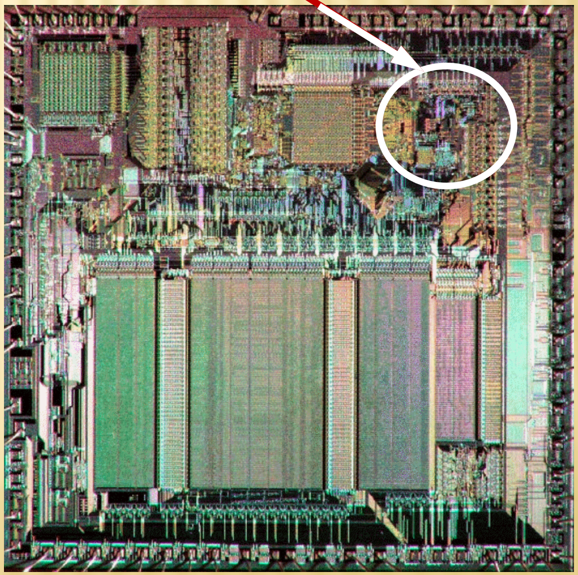
ISOCHRONOUS ZONE

Delay in any wire is less than the least delay of any library cell

In 1-μm and higher CMOS process



In deep submicron CMOS process



SPEED-INDEPENDENT CIRCUIT BASE PRINCIPLES

- Two-phase operation mode: working phase and spacer
- The use of dual-rail, biphasic and unary information signals
- Acknowledging the switching of all circuit cells by an additional indication subcircuit
- Handshake between subsequent functional blocks in the information processing path
- Unlimited circuitry basis

DELAY-INSENSITIVE CIRCUIT BASE PRINCIPLES

NULL Convention Logic (NCL) is a typical representative of the DI circuits

- **Two-phase operation mode: working phase and spacer**
- **The use of dual-rail only information signals**
- **Each cell indicates all own inputs**
- **Limited multi-threshold cell library (29 cells)**

SI AND NCL CIRCUITS COMPARISON

	SI circuits	NCL circuits
Advantages	✓ Less complexity (up to 2 times for combinational circuits and up to 4 times for sequential ones) ✓ Unlimited cell basis ✓ Analysis software	✓ Simple indication (only circuit outputs should be indicated) ✓ Easier design automation (BALSA, UNCLE)
Drawbacks	▪ Additional indication subcircuit controlling all circuit cells ▪ Hard formalization for design automation	▪ Large complexity both of combinational and sequential circuits ▪ Less performance ▪ Larger power consumption

SOFTWARE FOR SI CIRCUIT DESIGN DEVELOPED IN FRC “CSC”

Self-timing properties analysis:

- Library cell level analysis (BTRAN, ASIAN)
- Functional block level analysis (ASPECT)
- VLSI level hierarchical analysis (LIMAN)

SI circuit synthesis:

- Custom and gate arrays base
- Industrial standard cell libraries extended by self-timed combinational and sequential cells

SI CIRCUIT EXAMPLES: MICRO CORE

Instruction Set:

MUL – multiply 4×4

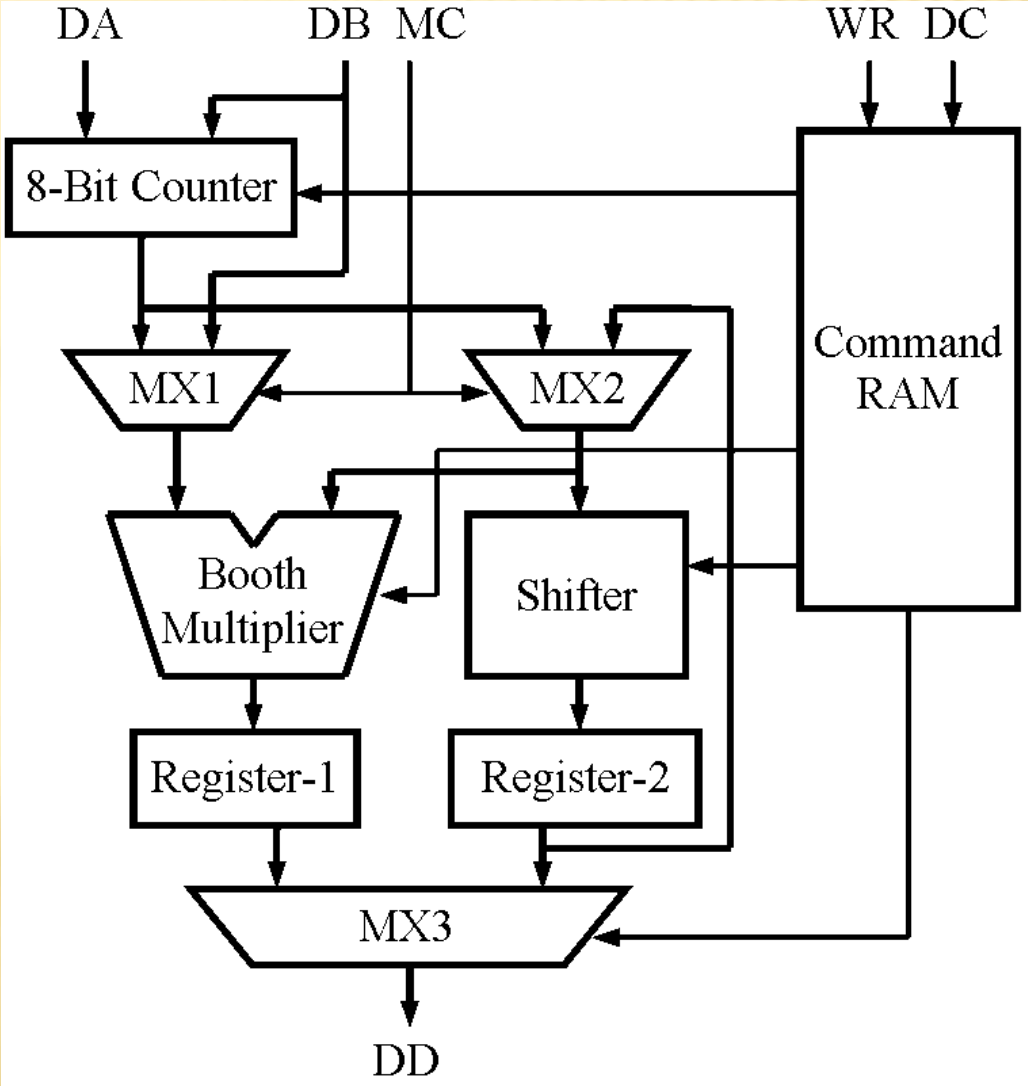
ROT – cyclic shift

JUMP – unconditional jump

NOP – no operation

CMOS Process

- **1.6 μm**
- **1 metal, 1 polysilicon**
- **Gate Array**



SI CIRCUIT EXAMPLES: MICRO CORE

Operation cycle duration for command sets

	Operation set	Synchronous, ns	Speed-independent, ns		
		typical	worst	typical	best
1	Cyclic MUL	250	166	144	118
2	Cyclic ROT	250	121	102	86
3	Cyclic NOP	250	111	93	75
4	Cyclic JUMP	500	90	78	66
5	MUL + JUMP + NOP + ROT	1248	516	440	364

SI CIRCUIT EXAMPLES: MICRO CORE

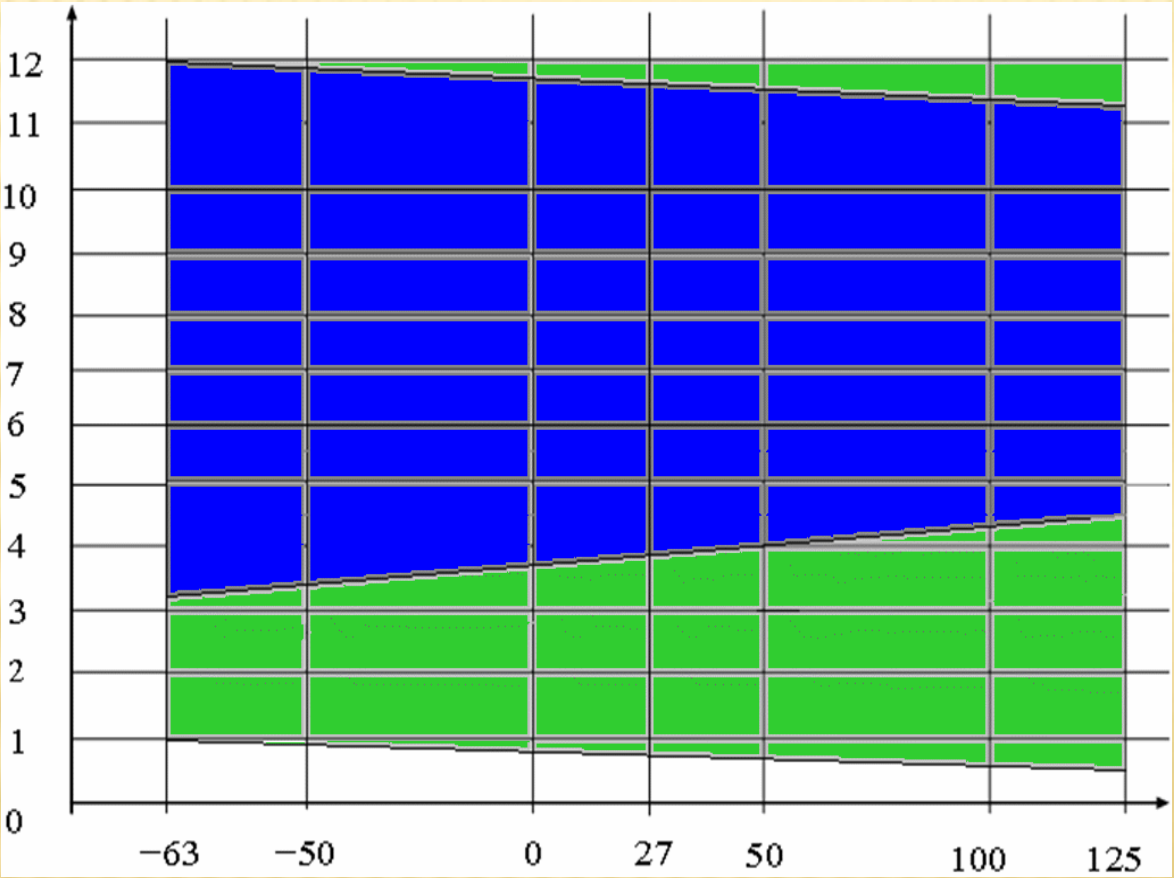
Hardware complexity on Gate Array basis

	Hardware	Synchronous, gates	Speed-independent, gates
1	Multiplier	177	444
2	Shifter	52	214
3	Counter	88	159
4	Command RAM	230	192
5	Control unit	423	380
	Total	970	1389

SI CIRCUIT EXAMPLES: MICRO CORE

Workability region

U_{DD}, V

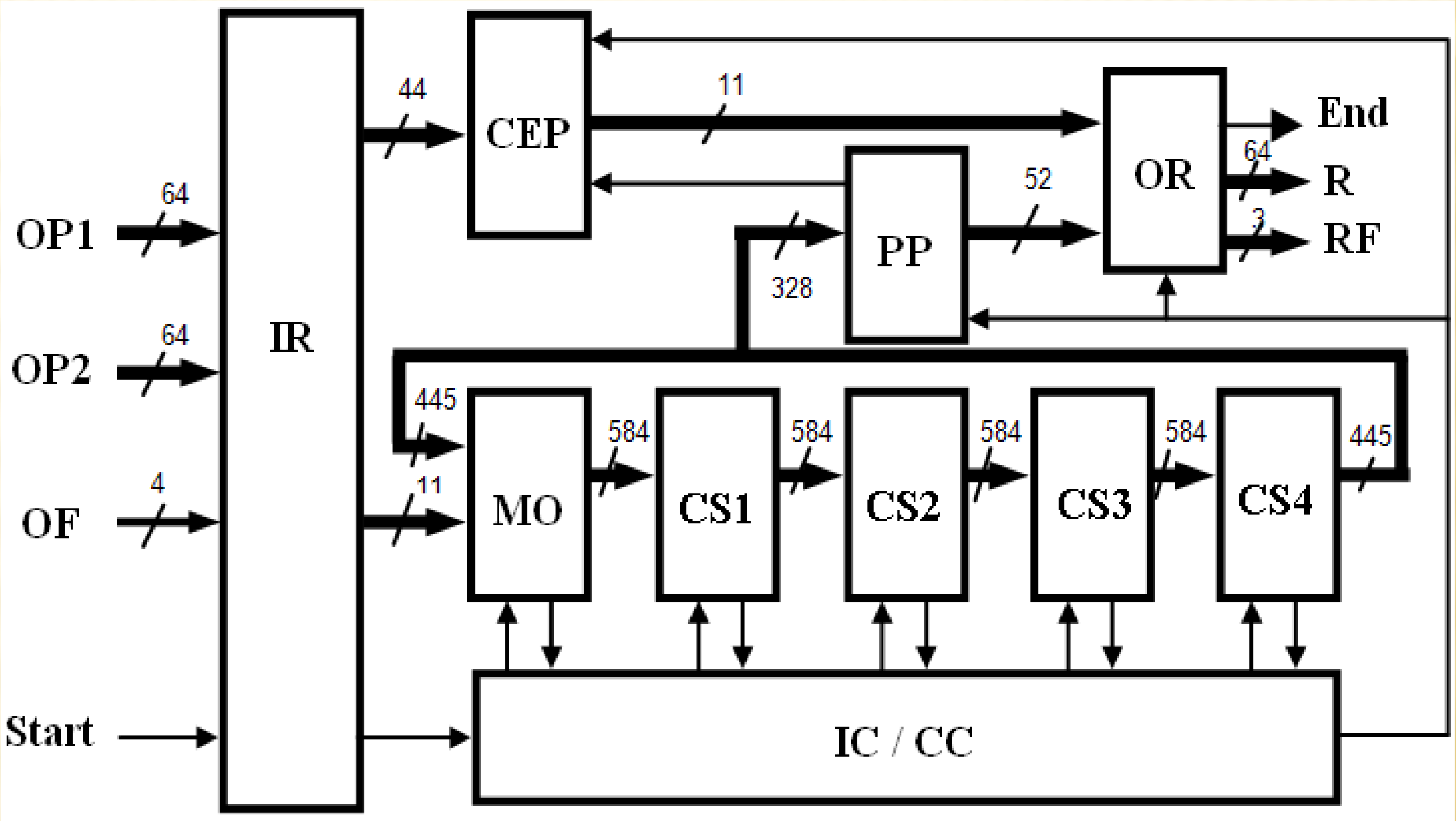


Synchronous

Speed-independent

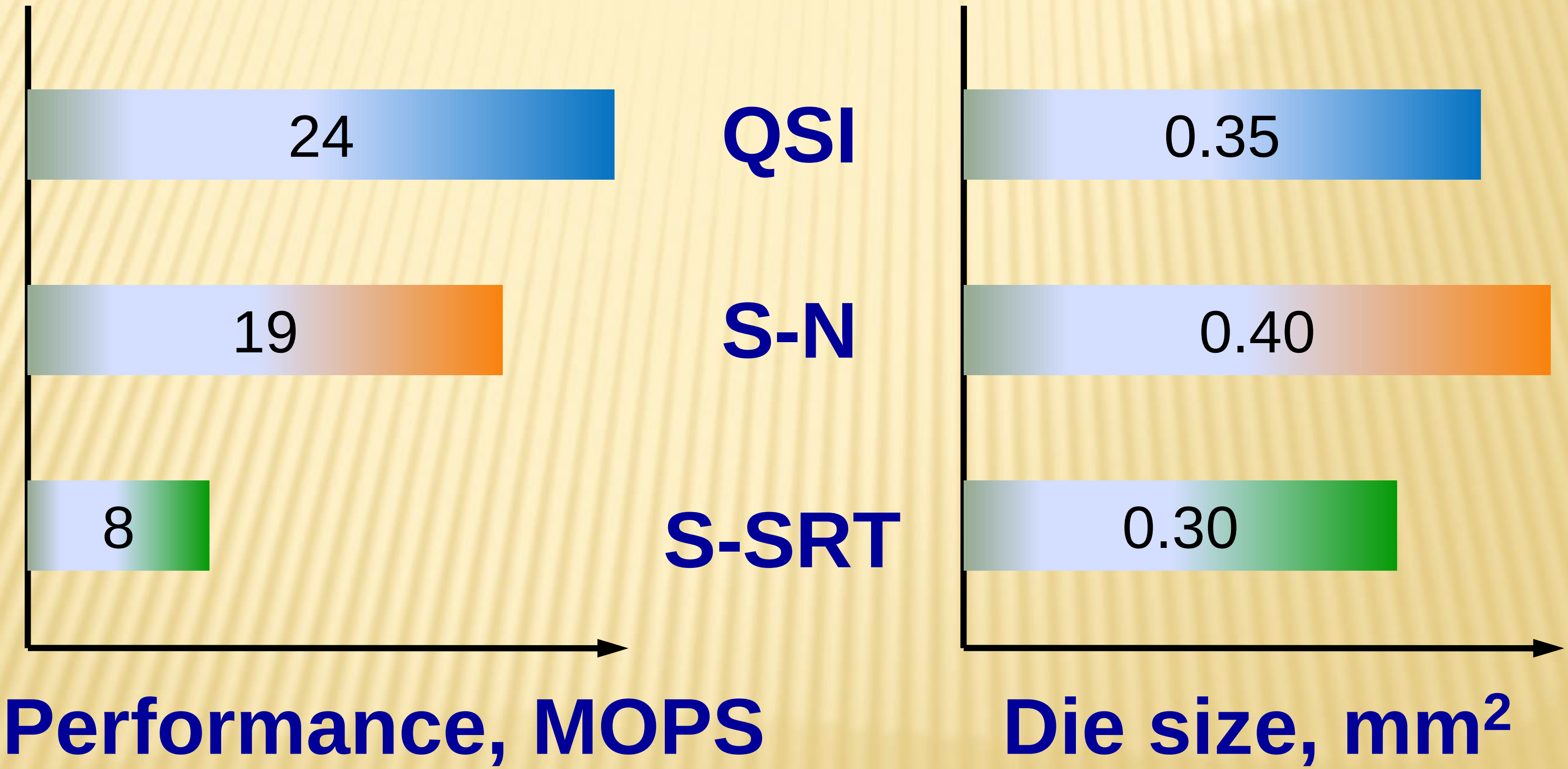
T, °C

SI CIRCUIT EXAMPLES: COPROCESSOR



SI CIRCUIT EXAMPLES: COPROCESSOR

Manufactured cases comparison



SI CIRCUIT EXAMPLES: COPROCESSOR

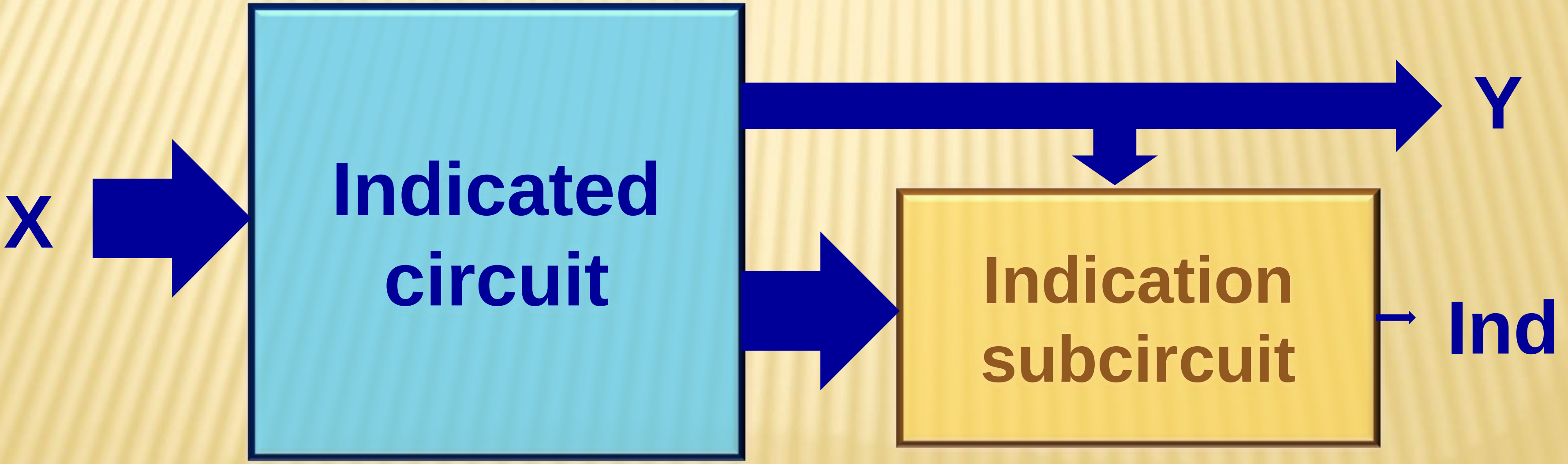
QSI and SI cases' performance, ns

	Conditions		QSI case		SI case	
	U_{DD}, V	T, °C	DIV	SQRT	DIV	SQRT
1	1.98	–63	34.7	36.9	47.3	50.2
2	1.80	25	46.7	49.1	63.5	67.0
3	1.62	125	63.9	70.3	86.9	90.1
4	0.32	125	25 688	25 301	34 940	34 410
5	0.20	125	-	-	340 800	336 920

SI CIRCUIT STRUCTURE

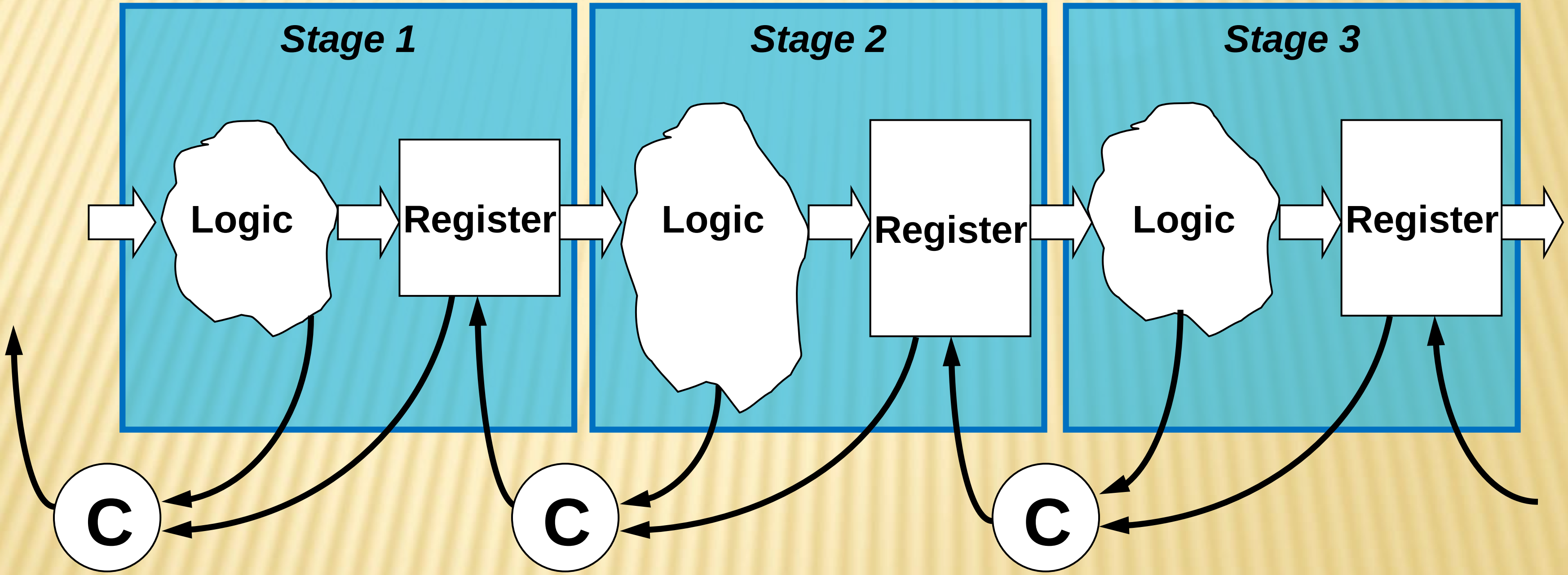
Factors limiting performance:

- Two-phase operation discipline
- An indication subcircuit acknowledging switching completion into the current phase

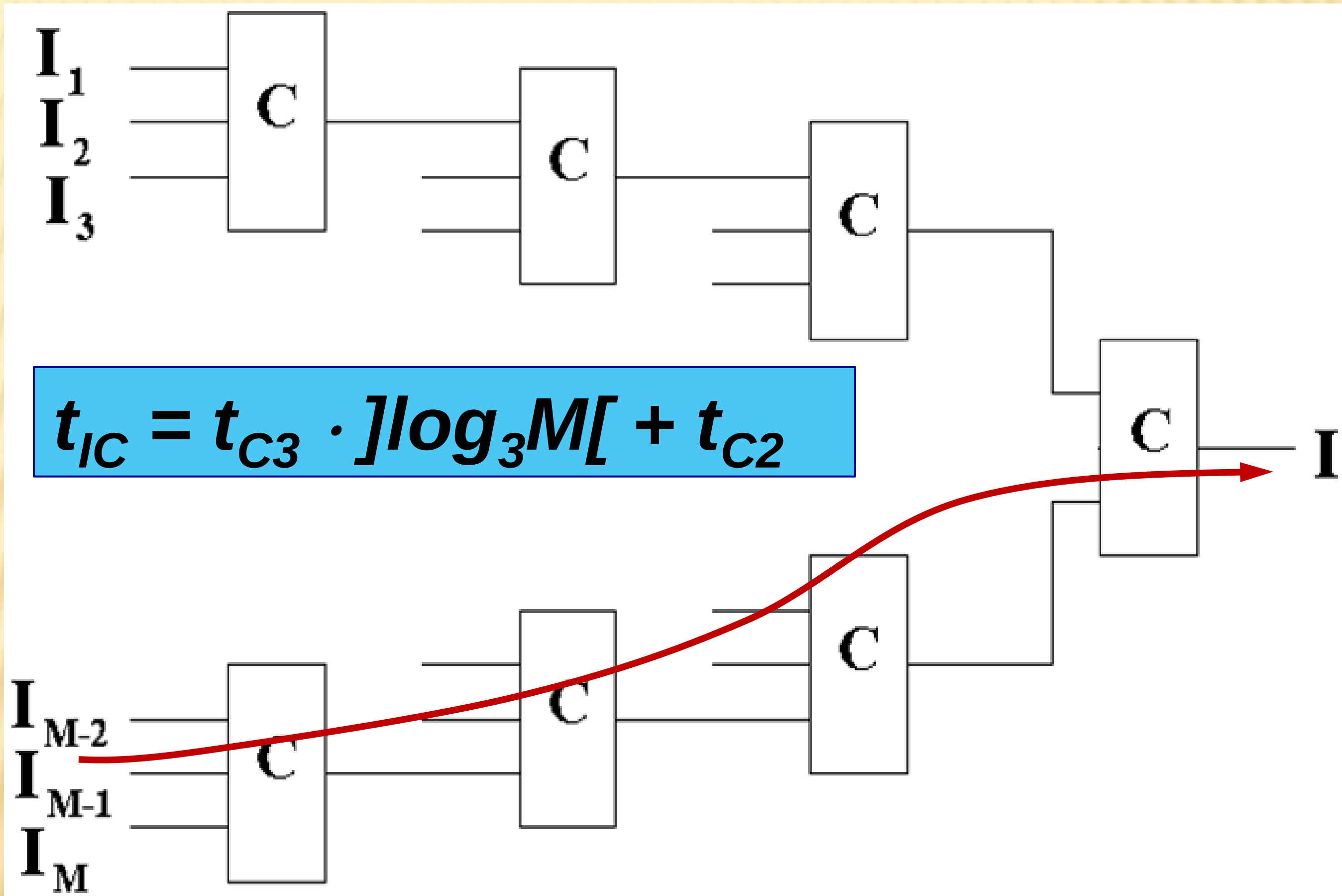


SI CIRCUIT PIPELINE

Traditional indication

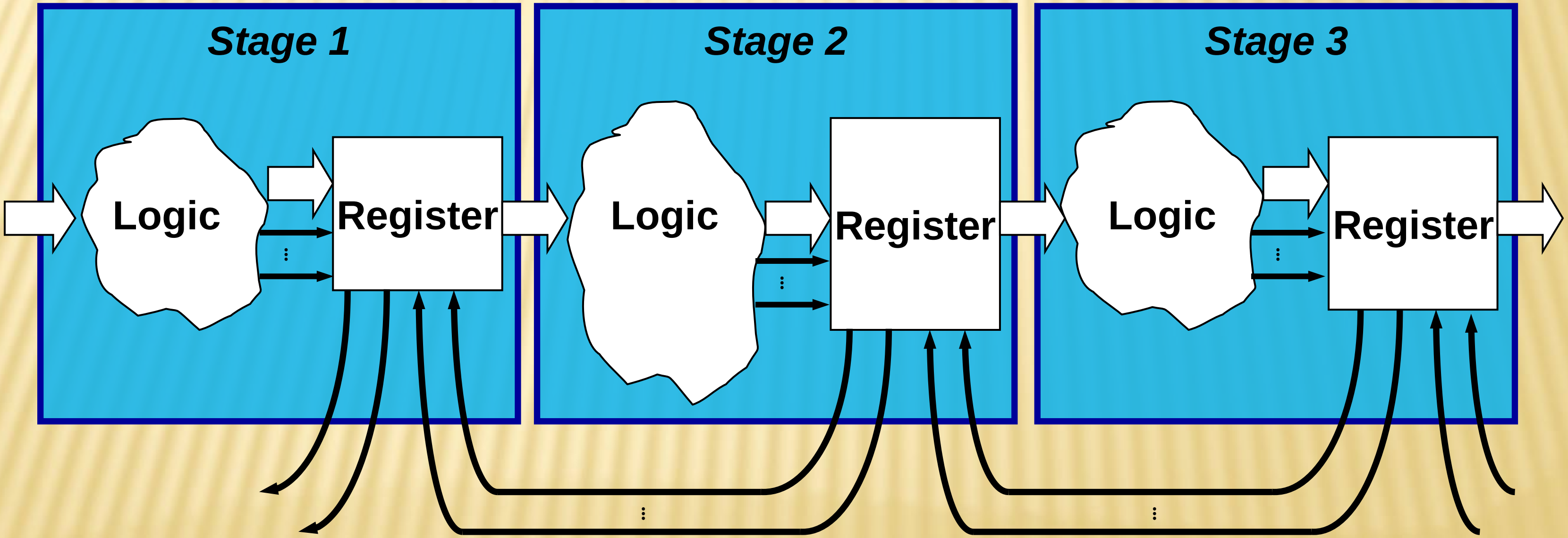


INDICATION SUBCIRCUIT STRUCTURE



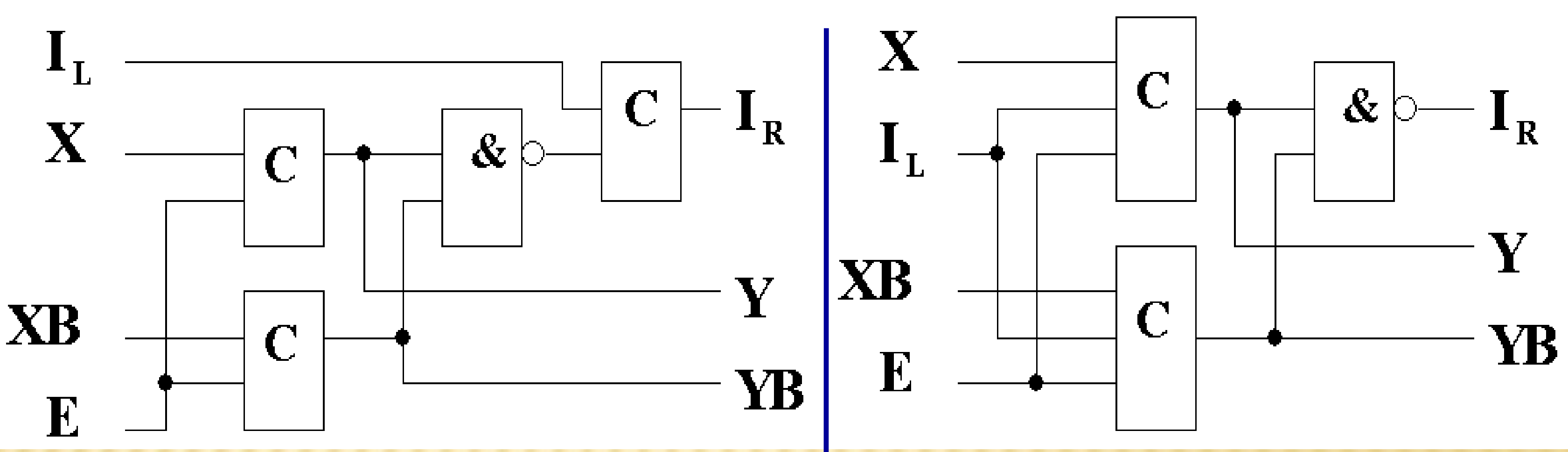
INDICATION SUBCIRCUIT OPTIMIZATION

- Bitwise indication of the Logic in the same stage Register
- Bitwise control of the previous stage Register



INDICATION SUBCIRCUIT OPTIMIZATION

- I_L is a bitwise indication output of the Logic
- I_R is a bitwise indication output of the Logic



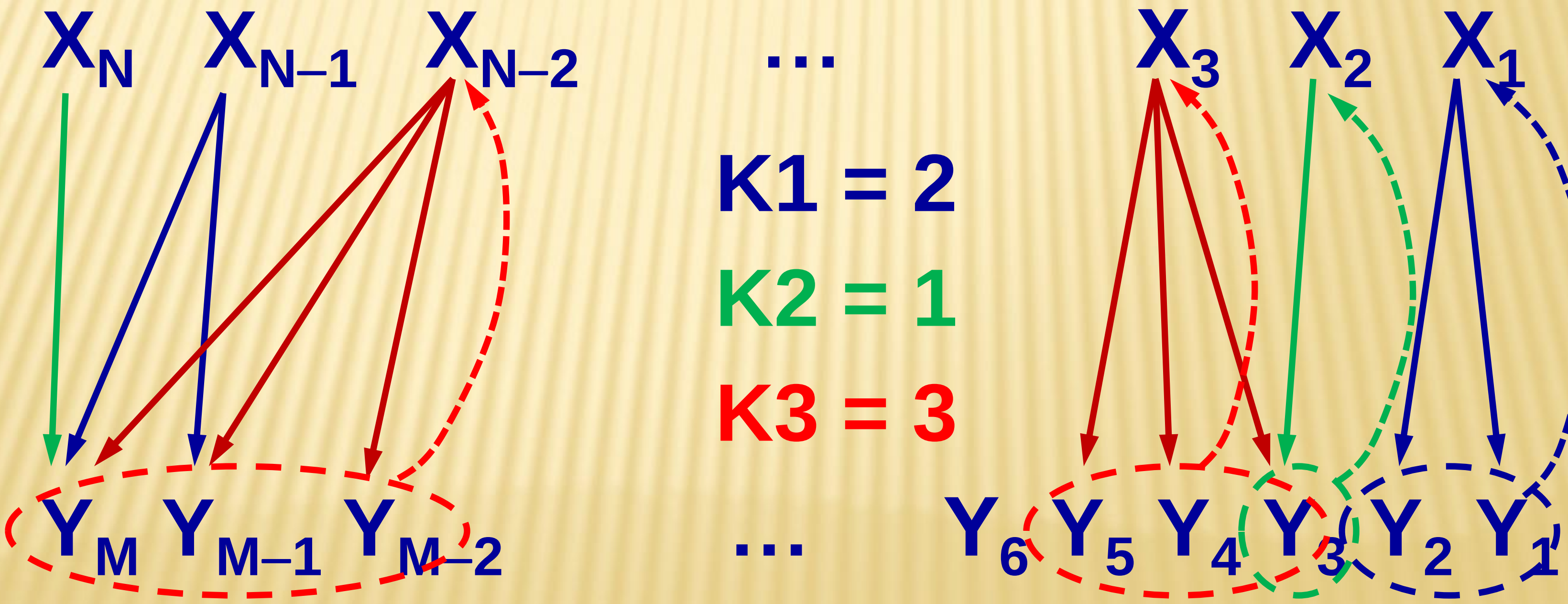
I_L delay is bigger than others input delays

I_L delay is close to others input delays

BITWISE INDICATION RULE

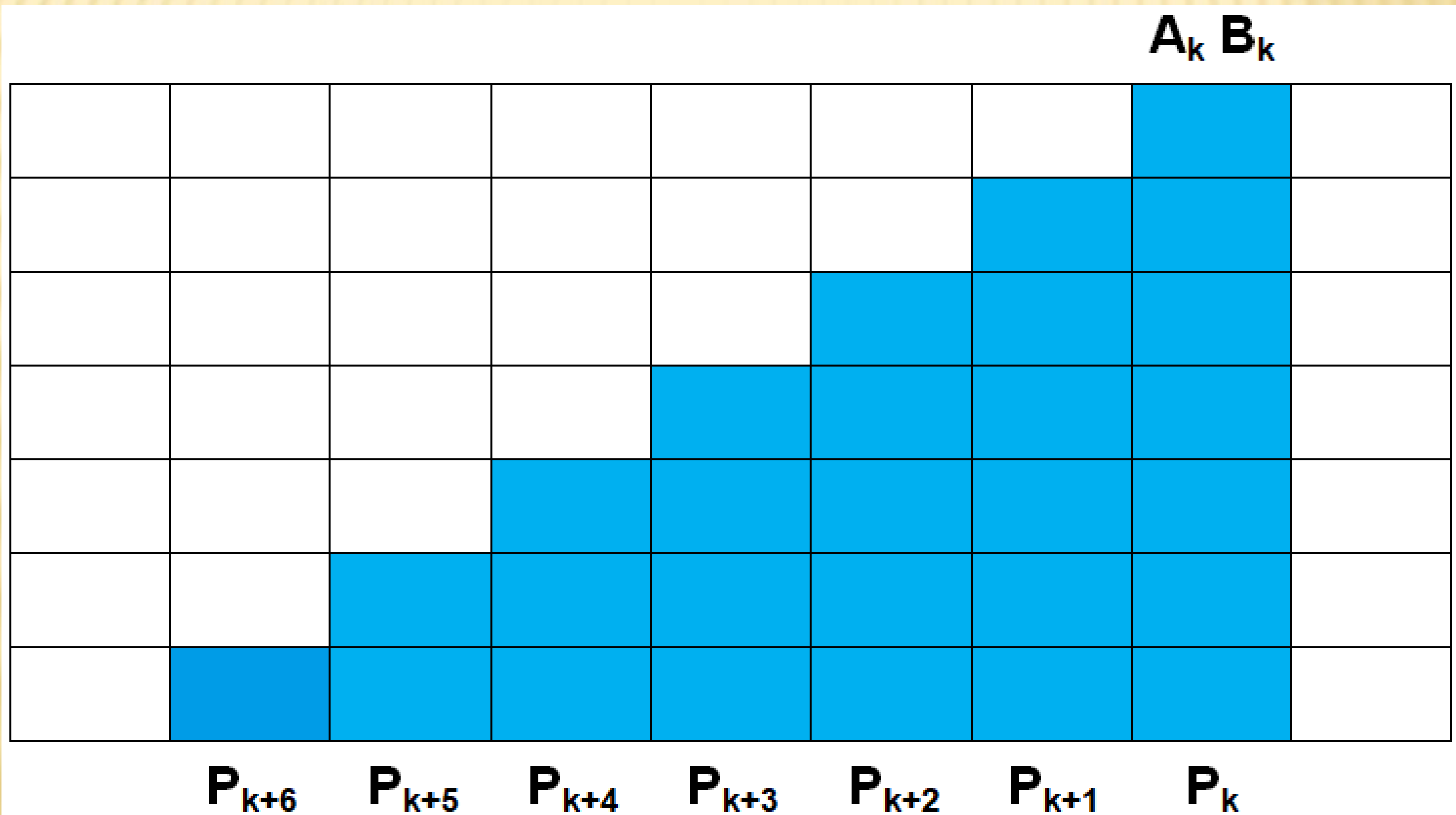
Each output controls only those inputs, which it depends on.

Connectivity coefficient "K":



WALLACE TREE BITWISE INDICATION

For one-stage 54-bit Wallace tree, K = 7

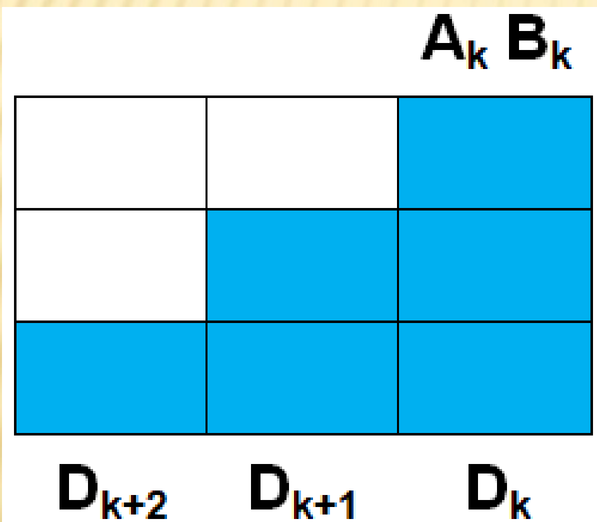


Layer 1
Layer 2
Layer 3
Layer 4
Layer 5
Layer 6
Layer 7

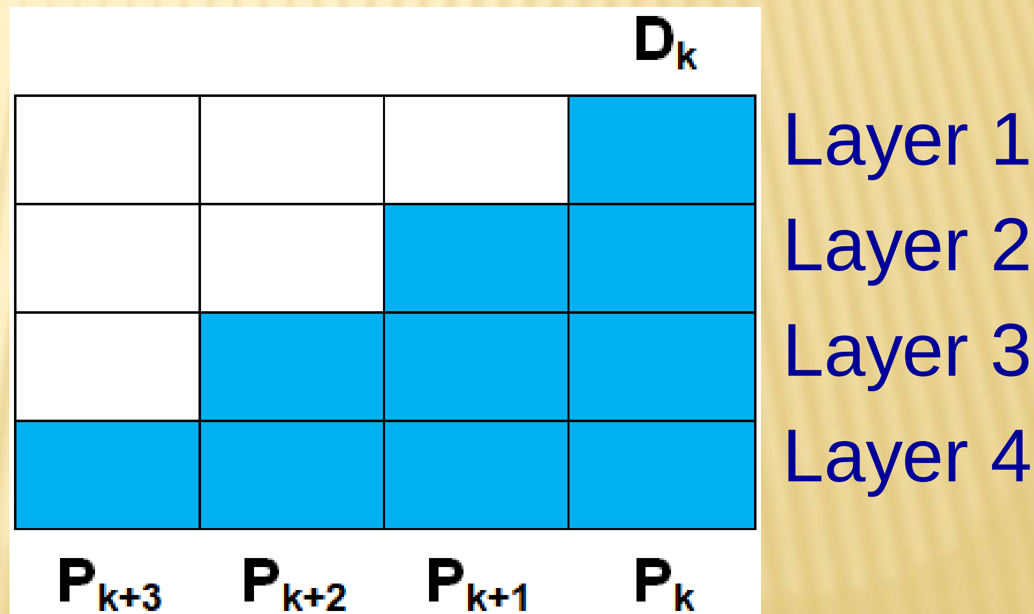
WALLACE TREE BITWISE INDICATION

For two-stage 54-bit Wallace tree:
$K_1 = 3; K_2 = 4$

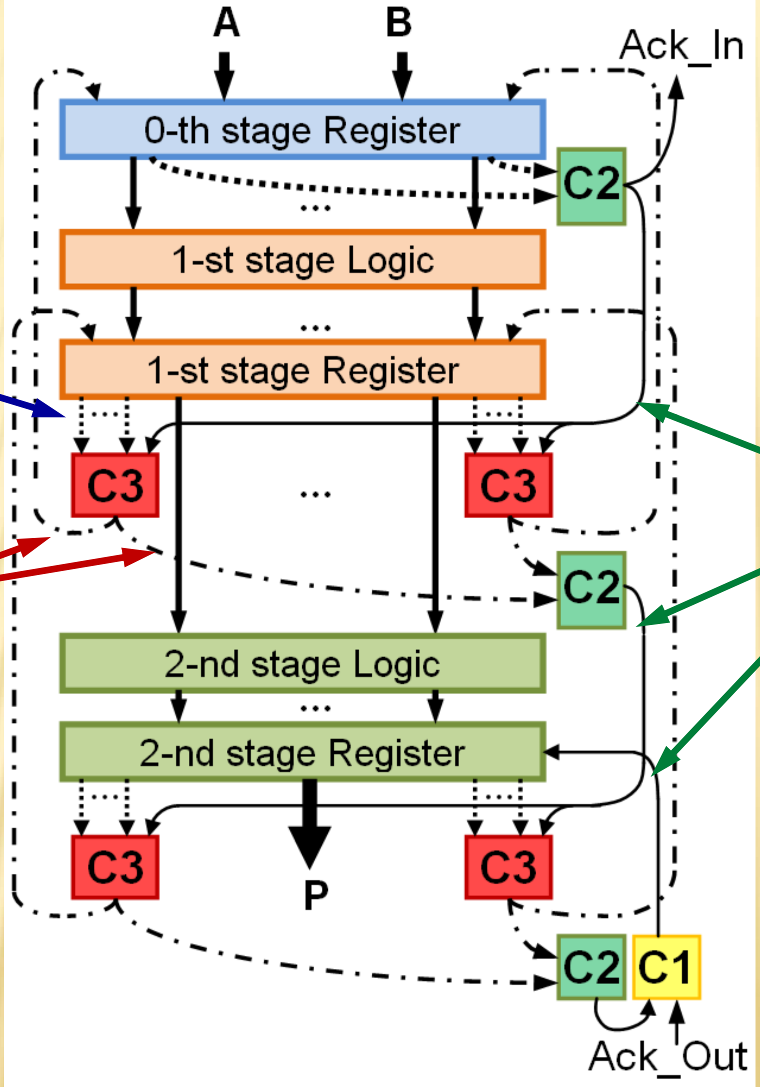
First WT stage



Second WT stage



WT'S PIPELINE BITWISE INDICATION



Bitwise indicators

Group indicators

Total indicators

WT'S PIPELINE BITWISE INDICATION

Simulation results and hardware estimates (65-nm bulk CMOS process)

Indication case	Average cycle duration, ps	Complexity, CMOS transistors
Classical	970	220 000
Bitwise & group	710	225 500

Self-timed circuits: Design methodology, Cell libraries, CAD tools, and Product prototypes

ST VLSI CAD

- ASPECT
- ASIAN
- FAZAN
- TASKAN
- SINTABIB
- SAMAN
- LIMAN

28 registered software tools

Functional description (VHDL, Verilog)

ST cell libraries

- GA 5503
- GA 5509
- GA 5521
- CMOS 180 nm
- CMOS 65 nm

37 RU patents
2 USA patents

Custom ST LSI & VLSI

- Microcontroller core (GA 5503)
- Codec (GA 5507)
- Arithmetic coprocessor IEEE 754 (180 nm)
- Arithmetic coprocessor IEEE 754 (65 nm)
- Fused Multiply-Add Unit IEEE 754 (65 nm)

Workability range increase (3-10 times); reduced power consumption (30-50%), increased performance (25-100%); constant fault detection (up to 100%)

CONCLUSIONS

- **Speed-independent (SI) circuitry is justified primarily in areas where high operational reliability is a determining factor**
- **Experimental results proved SI circuits advantages in the workability range and performance. In real conditions, typical computing speed-independent units with a low bit width of processed data have a better performance of 1.7 – 2.6 times than their synchronous analogs**
- **The use of bitwise or group indication and control in multi-bit SI circuits significantly accelerates their work at the expense of a relatively small increase in hardware complexity**

CONTACTS

- **Address: Institute of Informatics Problems, Federal Research Center "Computer Science and Control" of Russian Academy of Sciences, Russia, 119333, Moscow, Vavilov str., 44, building 2**
- **Director: academician Sokolov I.A.**
  - **Tel.: +7 (495) 137 34 94**
  - **Fax: +7 (495) 930 45 05**
  - **E-mail: ISokolov@ipiran.ru**
- **Speaker: Diachenko Y.G., YStepchenkov@ipiran.ru**

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