

System's Debugging Tools for Recurrent-Computing Device

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EXTENDED ABSTRACT

Keywords – data-flow architecture, debugging tools, recurrence.

For the developed hybrid recurrent signal processor, at a stage of approbation of architectural concepts and diagram implementation with programmed logic, the composition is revealed and the comparative analysis of system debugging instruments of a development environment of Quartus II is carried out. The powerful instruments of verification which are a part of this development environment, allow as reducing time of obtaining the ready project, and especially reducing expenses. On the basis of the comparative analysis and according to the selected criteria the composition of debugging tools of the recurrent calculator is defined. The optimum structure of hardware of debugging recurrent signal processor is offered. The most convenient tools using in system debugging of Quartus II development environment are defined. They allow for significant simplification of project verification process on the basis of the diagram with programmed logic in a real hardware surrounding. Debug means supporting an effective process of joint debugging hardware and software taking into account means of system debugging of a development environment of Quartus II are offered and implemented in the hybrid recurrent signal processor.

As a result, additional debugging resources were realized in hybrid recurrent signal processor such as mirror memory, step counter, register's contents memory, virtual keys, virtual indicators, and debug events handler. In aggregate with the built-in means of system debugging of Quartus II, they appeared to be enough for supporting an effective process of joint debugging hardware and software. According to chosen criteria of debugging, external additional equipment wasn't used. An assumption was proved that using compromise option (a combination of the built-in tools and additionally designed unique debugging facilities) will allow for optimizing time and financial costs of the debugging facilities realization. The principles which are the cornerstone of additionally developed debugging tools can be used not only for hybrid recurrent signal processor, but also for debugging devices within traditional architecture.

Reference to full text: <http://www.mes-conference.ru/infoMES/index.php?page=vpaper&code=D572&ls=en>

Problemi Razrabotki Perspektivnih Mikro- i Nanoelektronnih system (MES), 2014, no 2, pp. 39-44 (in Russian).

REFERENCES

- Volchek V.N., Stepchenkov Yu.A., Petrukhin V.S., Prokof'ev A.A., Zelenov R.A. Problemi Razrabotki Perspektivnih Mikro- i Nanoelektronnih system (MES), *IPPM RAN*, Moscow, 2010, pp. 412-417 (in Russian).
- Stepchenkov Yu.A., Petrukhin V.S. *Sistemy i sredstva informatiki*, 2008, issue ext., pp. 118–129 (in Russian).
- Volkov Dmitriy. *Otkrytye sistemy. SUBD*, 2006, no 5, p. 1 (in Russian).
- Leonid Chernjak. *Otkrytye sistemy. SUBD*, 2006, no 5, pp. 20-25 (in Russian).
- Stepchenkov Yu.A., Petrukhin V.S., Filin A.V. *Sistemy i sredstva informatiki*, 2001, issue. 11, pp. 283–315 (in Russian).
- Stepchenkov Yu.A., D'yachenko Yu.G., Petrukhin V.S., Filin A.V. *Sistemy i sredstva informatiki*, 1999, issue 9, pp. 261–292 (in Russian).
- P. Beerel, J. Cortadella, and A. Kondratyev, "Bridging the gap between asynchronous design and designers (Tutorial)," in *VLSI Design Conference*, (Mumbai), 2004.
- Anant Agarwal, Ben-Hong Lim, David Kranz, and John Kubiawicz. *APRIL: A processor architecture for multiprocessing. Proc. 17th Annual Intl. Symp. on Computer Architecture*, Seattle, Washington, U.S.A., May 28-31, 1990, pp. 104-114.
- Volchek V.N., Zelenov R.A., Prokof'ev A.A. Problemi Razrabotki Perspektivnih Mikro- i Nanoelektronnih system (MES), *IPPM RAN*, Moscow, 2012, pp. 137-142 (in Russian).
- Shneider A.U., Petrukhin V.S., Stepchenkov Yu.A. Problemi Razrabotki Perspektivnih Mikro- i Nanoelektronnih system (MES), *IPPM RAN*, Moscow, 2012, pp. 133-136 (in Russian).
- Katalog oborudovaniya. 2012-2013, pp. 386–395, available at: http://www.tehencom.com/Companies/Tektronix/Tektronix_Catalog_2012_Rus.pdf (accessed 28.01.2014).
- About Excalibur Embedded Processor solutions.. available at: <http://www.altera.com/products/devices/excalibur/exc-index.html/> (accessed 27.02.2014).
- Stepchenkov Yu.A., Petrukhin V.S. *Metody i sredstva razrabotki informacionno-vychislitel'nyh sistem i setej*, 2004, special no. pp 89-133 (in Russian).
- Cyclone V GX FPGA Development Board Reference Manual. available at: http://www.altera.com/literature/manual/rm_cvgx_fpga_dev_board.pdf (accessed 28.01.2014).
- Petrukhin V.S., Volchek V.N., Prokof'ev A.A., Zelenov R.A. *Sistemy i sredstva informatiki*, 2008, issue ext., pp. 130–148 (in Russian).
- Petrukhin V.S., Hil'ko D.V. *Sistemy i sredstva informatiki*, 2008, issue ext., pp. 149–158 (in Russian).
- Quartus II Handbook Version 12.0. Volume 3: Verification. Altera. 101 Innovation Drive San Jose, CA 95134. www.altera.com. QII5V3-12.0.0. available at: http://www.altera.com/literature/hb/qts/quartusii_handbook.pdf (accessed 28.01.2014).
- Antonov Aleksandr, Filippov Aleksej, Zolotuh Roman. *Komponenty i tehnologii*, 2008, no 12 (in Russian), available at: http://kit-e.ru/articles/plis/2008_12_53.php
- Grebennikov A. *Sovremennaja Jelektronika*, 2010, no 9 (in Russian), available at: <http://www.soel.ru/issues/?id=343889> (accessed 05.012.2013).
- Grushvickij R., Mihajlov M. *Komponenty i tehnologii*, 2007, no 9 (in Russian), available at: http://kit-e.ru/articles/plis/2007_09_133.php (accessed 05.12.2013).