Yury Stepchenkov, Dmitry Khilko,
Yury Shikunov, Georgy Orlov

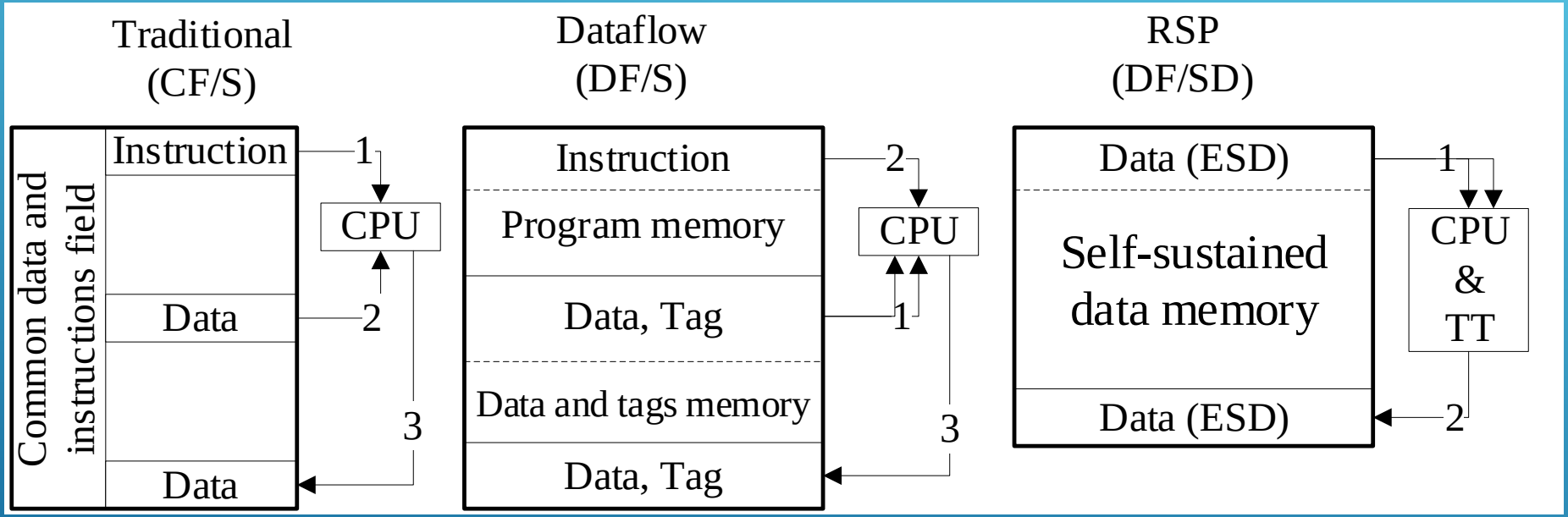
TESTING AND OPTIMIZATION OF RECURRENT SIGNAL PROCESSOR

Institute of Informatics Problems, Federal Research Center "Computer Science and Control" of the Russian Academy of Sciences, (IPI FRS CSC RAS), IPI RAS

The research was funded by a grant from the Russian Science Foundation (Project № 19-11-00334).

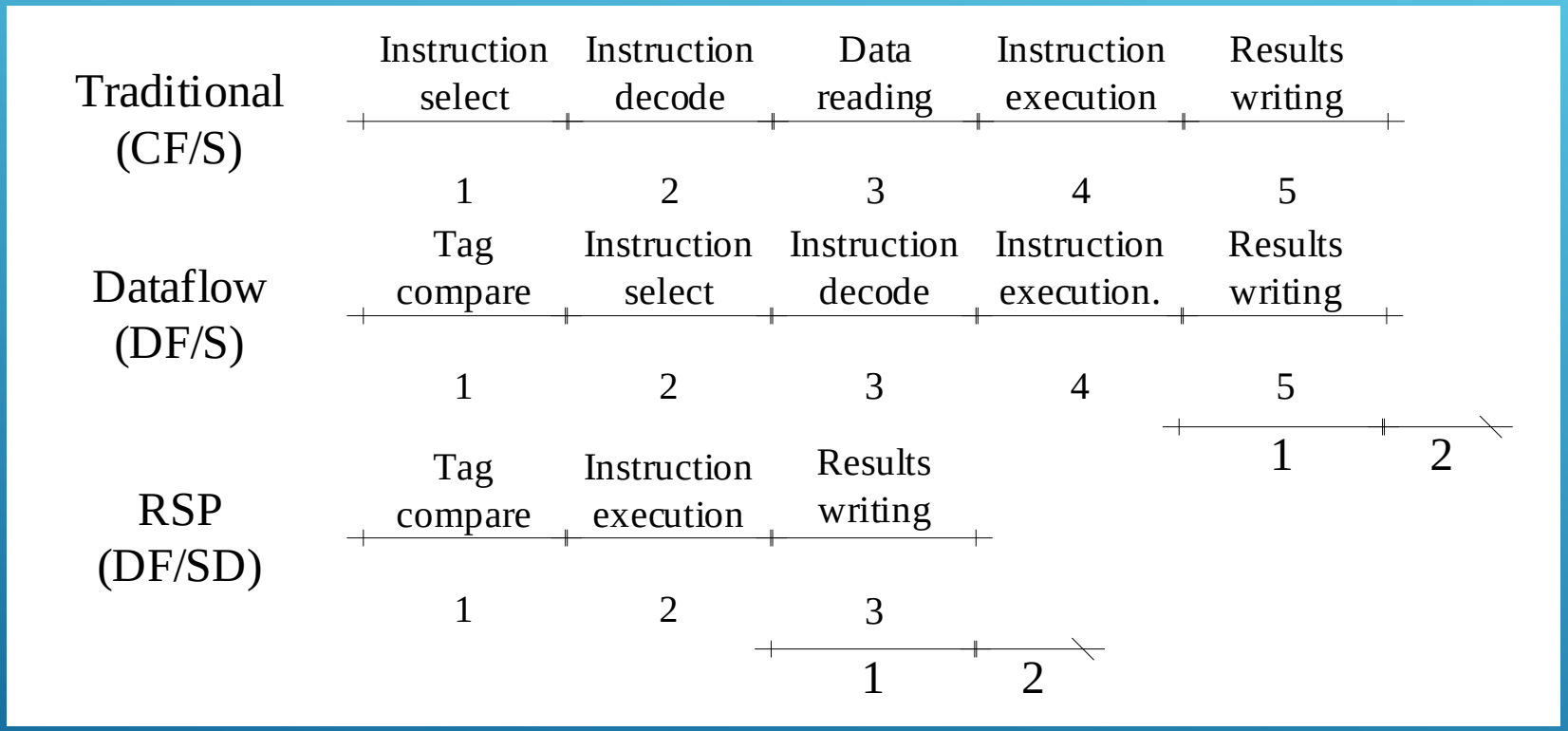
Moscow, 2020

KEY DIFFERENCES BETWEEN RSP AND EXISTING ARCHITECTURES



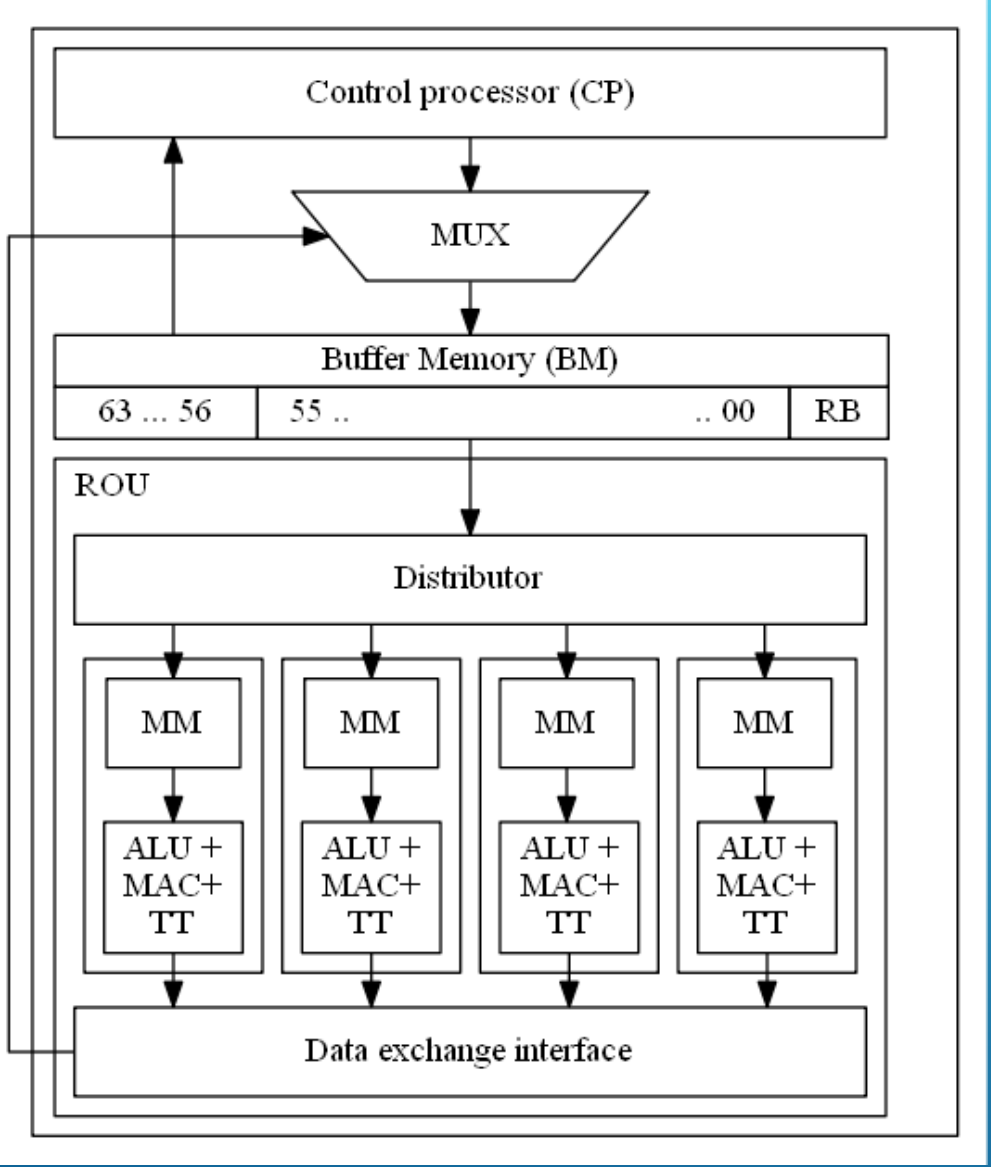
Main criteria – Instruction flow memory organization: *Control-Flow/Static (CF/S), Data-Flow/Static (DF/S), Data-Flow/Static-Dynamic (DF/SD)*

KEY DIFFERENCES BETWEEN RSP AND EXISTING ARCHITECTURES



Main criteria – logical steps needed to perform instruction

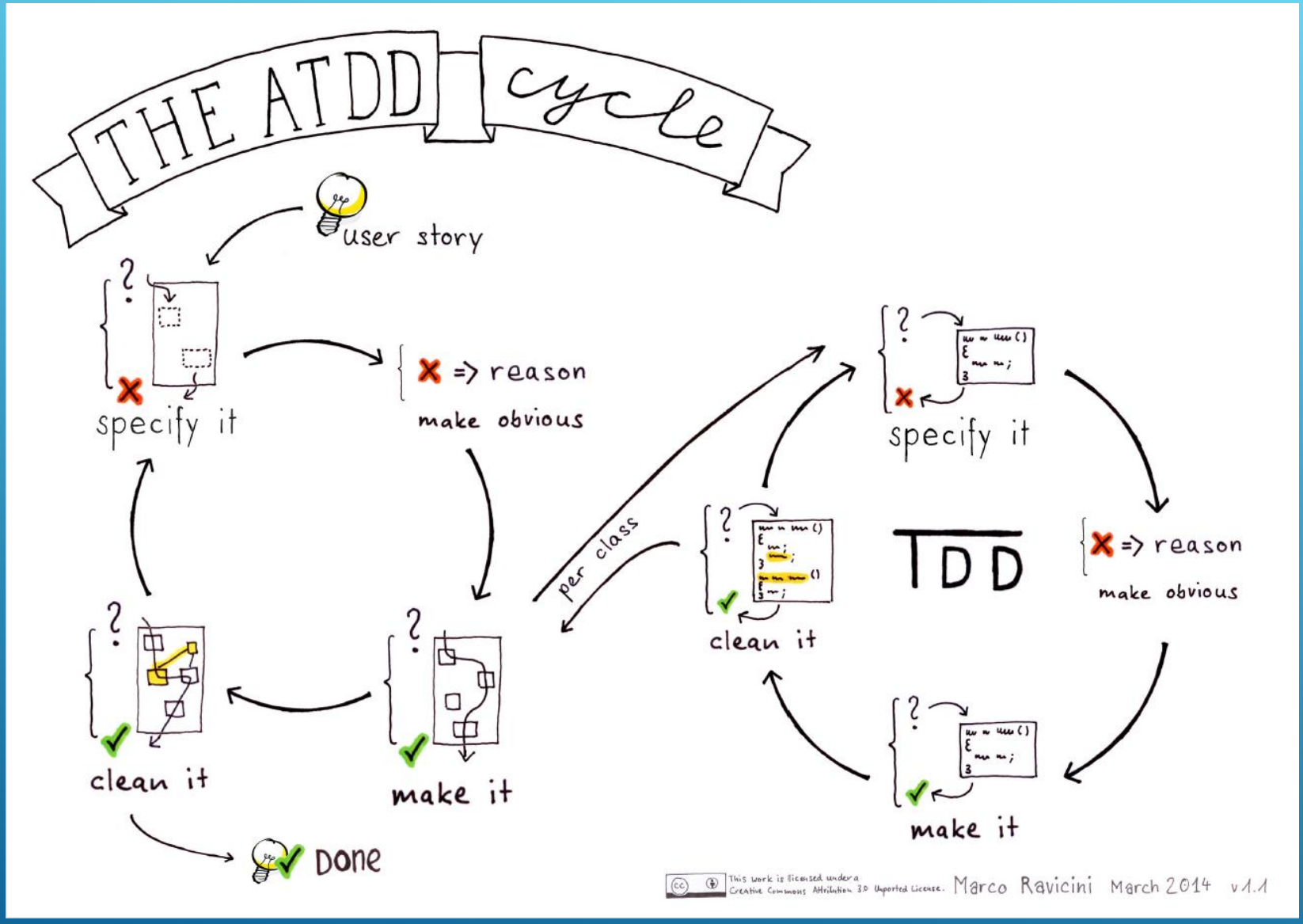
HYBRID PROTOTYPE ARCHITECTURE



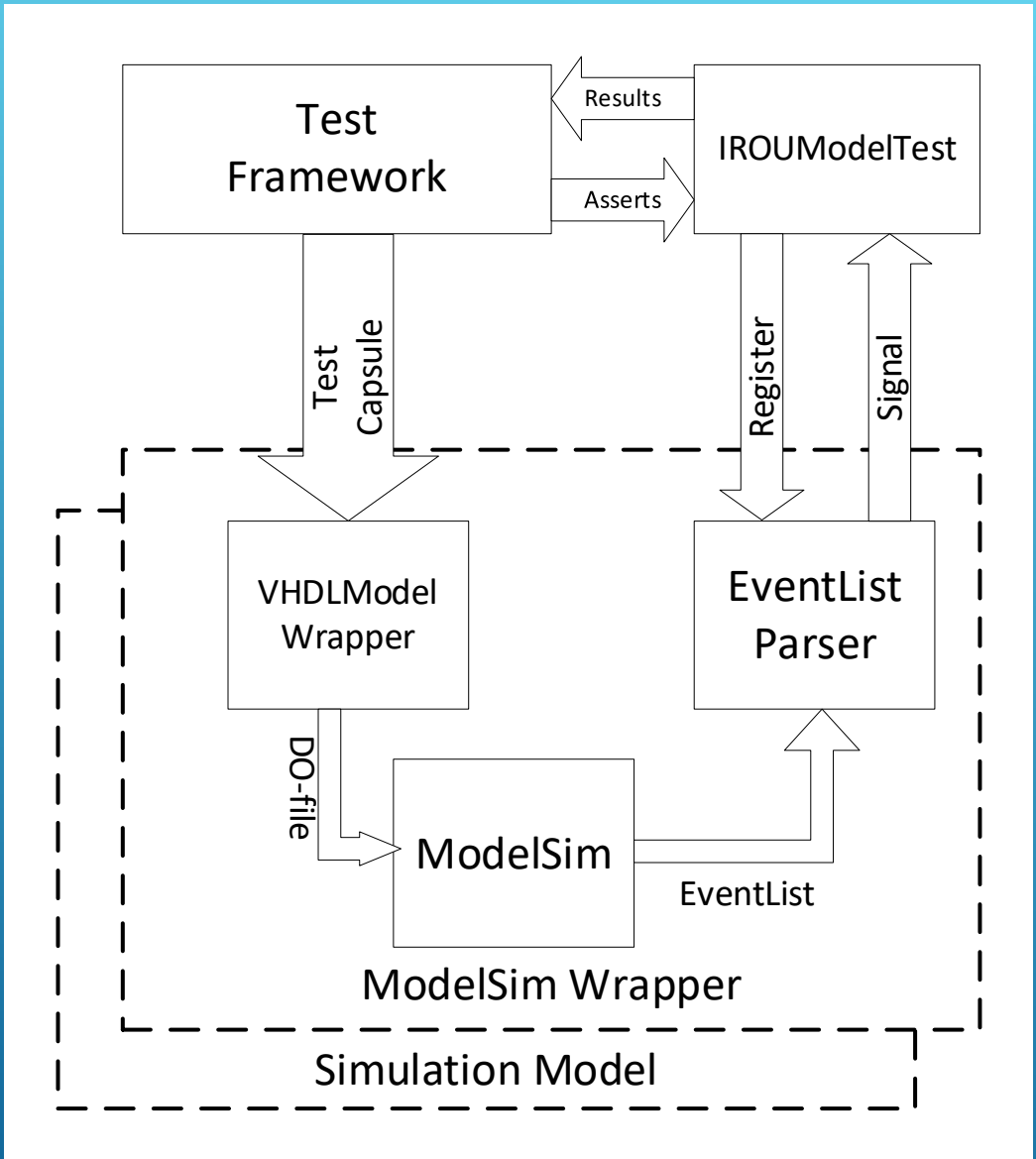
- MM is a match memory;
- MAC - Multiplier Accumulator;
- TT - tag transformer;
- RB - data readiness bit.

MAC, ALU and TT form the basis of the "Computer" component of the model.

TEST-DRIVEN DEVELOPMENT



VHDL MODEL TEST FRAMEWORK

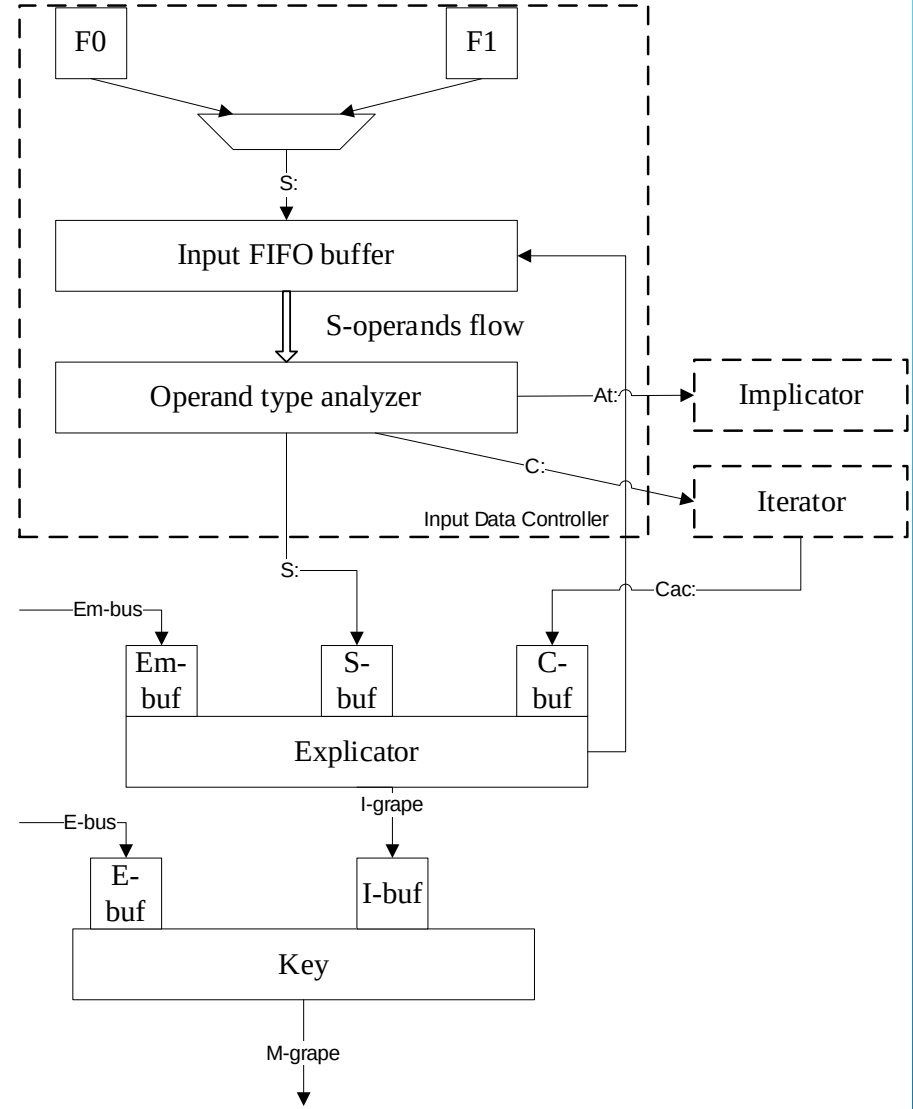


INITIAL STAGE PERFORMANCE

Performance estimation results has been obtained with Visual Studio 2019 Community Edition profiling tools

Stage	Total Time, ms	Multiplier	Time per Section, ms	Load Ratio
Distributor	1558.87	1	1558.87	1
MM	1429.85	0.25	357.46	0.23
Computer	2190.59	0.25	547.65	0.35

DISTRIBUTOR ARCHITECTURE



DISTRIBUTOR PERFORMANCE

Action	Total Time, ms
CallBS	22.94
Configure	5.32
Hold[a]	0
Init	8.91
ReadFReg	3.90
Resume[a]	0
Start	24.47
Stop[a]	0
Terminate	0.31
UnPack	175.68
WriteFIFO	1.26
WriteFReg	4.25
WriteToBranchMemory[b]	0
IDC	247.04
ReadFIFO	8.73
AddToGrape1	634.84
AddToGrape2	237.46
Explicator	881.03
MergeElGrapes	425.58
Step	5.22
Key	430.80

Distributor is implemented as a discrete event model. That is, it has a set of 10 states and a set of 18 actions that provide a transition between these states.

OPTIMIZATION RESULTS

- The Distributor stage was split into the IDC-Explicator-Key stage and the system has become relatively well balanced.

Stage	Total Time, ms	Multiplier	Time per Section, ms	Load Ratio
IDC	247.04	1	247.04	0.28
Explicator	881.03	1	881.03	1.00
Key	430.80	1	430.80	0.49
MM	1429.85	0.25	357.46	0.41
Computer	2190.59	0.25	547.65	0.62

FURTHER RESEARCH

The next optimization would be to split the Explicator into two steps.

VHDL and Simulation models equivalence have been proven on a set of test capsules covering the majority of the architecture specification.

This equivalence allows us to synthesize the FPGA prototype that will function identical to the simulation model, while retaining flexibility associated with software development.

THANK YOU FOR YOUR ATTENTION!

CONTACTS

- Director: academician Sokolov I.A.
- Address: Institute of Informatics Problems of the Federal Research Center "Computer Science and Control" of the Russian Academy of Sciences (IPI RAS), Moscow, Russian Federation, 119333, Vavilova str., 44, b.2
- Tel: +7 (495) 137 34 94
- Fax: +7 (495) 930 45 05
- E-mail: ISokolov@ipiran.ru

- Stepchenkov Y.A., tel. +7 (495) 671 15 20, Ystepchenkov@ipiran.ru