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Failure-Tolerant Synchronous and Self-Timed Circuits Comparison

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Abstract—The article considers the problem of developing synchronous and self-timed (ST) digital circuits tolerant to soft errors. Synchronous circuits traditionally use the "2-of-3" voting principle to ensure a single failure, resulting in three times the hardware costs. Due to dual-rail signal coding and two-phase control in ST circuits, duplication provides a soft error tolerance level 2.1 to 3.5 times higher than the triple modular redundant synchronous counterpart. The development of new high-precision software simulating microelectronic failure mechanisms will provide more accurate estimates for the electronic circuits' failure tolerance.

Keywords: synchronous circuit, self-timed circuit, soft error, failure tolerance, triple modular redundancy, duplication, reliability

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1. INTRODUCTION

Masking soft errors that occur due to the impact of nuclear particles, electromagnetic pulses, noise pick-ups, and other causes is an essential task in solving the problem of electronic equipment reliability. A soft error is a change in the cell output's logical state caused by a single event that does not lead to its active components' fault [1].

Soft error detection and masking in synchronous circuits are provided using fault-tolerant codes [2] or simultaneous processing of input data by several parallel identical channels with subsequent voting of the correct result [3]. Failure-tolerant code fends off a limited subset of soft errors. With an increase in the density of transistors on the chip area, the practicality of its use decreases due to the appearance of multiple failures when exposed to a single cause, which this implemented code cannot cover.

The voting principle provides reliable masking of any number of failures that occur in a minor subset of channels. Usually, the "2-of-3" principle [3] is used, which guarantees reliable circuit operation under conditions when no more than one soft error is observed at any given time. With a higher intensity of failures, there is a possibility of a simultaneous failure in two or more of the three channels, leading to a critical error.

The undoubted advantage of the tripled circuit is the decision-making "on the fly" and the continuation of correct operation in the event of a single soft error in any channel. It also protects against multiple failures in a single channel.

Due to the two-phase operation mode and the completion detection of switching to the current phase, self-timed (ST) digital circuits [4] have behavior independent of cell delays and higher natural tolerance to soft errors [5, 6] than their synchronous counterparts. Paper [7] proposed methods for increasing the ST circuit's soft error tolerance. However, they do not provide complete protection against them.

This article studies the possibilities and methods for constructing one hundred percent soft-error-tolerant ST circuits and their comparison with synchronous counterparts.

2. ENSURING SOFT ERROR TOLERANCE OF ST CIRCUITS

The functional correctness of ST circuit operation at any generation and propagation delays of internal and output signals is the primary advantage of actual ST circuits. Monitoring the completion of switching all circuit cells to the next operation phase provides such a feature. Reducing the supply voltage and increasing the ambient temperature slows down the ST circuit's operation but does not corrupt the correctness of the data processing algorithm performed by the circuit. The independence of cell delays makes it possible not to focus on the worst case and provides a temporary suspension of the ST circuit operation until the end of a detected soft error. But the convenient ST circuits detect not all soft error types.

The easiest way to ensure that the ST circuit masks all soft errors is ST circuit duplication [8], shown in the Fig. 1. Two identical channels process the same

D_{in} input. Voting circuit "1-of-2" compares their information outputs D_1 and D_2 and chooses the correct result D_{out}. It directs channel output D_1 to the output D_{out} during failure-free operation. The indication outputs of channels I_1 and I_2 are flags of the channel outputs' readiness. The Req input enables the transition of this ST into the next phase of operation, and the Ack output acknowledges the successful completion of this ST circuit transition into the current phase.

The appropriate layout design of the ST circuit ensures protection against the soft error of the "incorrect working state" type [6]. Then a bitwise comparison of the outputs D_1 and D_2 guarantees the soft error detection as the state that does not correspond to the current ST circuit phase.

The duplicated ST circuit has two sources, which can indicate the result's correctness. They are two information output sets and two indication outputs. If they match in pairs, then both circuit's halves coincide. Otherwise, some channel has not yet finished switching, or a soft error occurred somewhere.

Let us compare the probabilities of a soft error in a synchronous and ST circuit, assuming that the likelihood of a failure is directly proportional to the circuit's die area, and hence to the number of transistors in it.

3. COMPARISON OF CONVENTIAL CIRCUITS

The soft error intensity λ in a conventional circuit that does not use the voting result can be estimated by the formula [3]:

$$\lambda = N\lambda_0\alpha,$$

where N is the number of transistors in the circuit; λ_0 is the flux density of random events (number of events per unit of time) initiating a failure in one transistor; α is the failure probability if one transistor is affected. Then the ratio K_I of failure intensities of the synchronous circuit and its ST counterpart equals:

$$K_I = \frac{\lambda_S}{\lambda_{ST}} = \frac{N_S\lambda_0\alpha_S}{N_{ST}\lambda_0\alpha_{ST}} = \frac{N_S\alpha_S}{N_{ST}\alpha_{ST}} = \frac{\alpha_S}{A_R\alpha_{ST}}, \quad (1)$$

where λ_S is the failure rate of the synchronous circuit; λ_{ST} is the failure rate of the ST circuit; N_S is the number of transistors in the synchronous circuit; N_{ST} is the number of transistors in the ST circuit; α_S is the failure probability if one transistor of the synchronous circuit is affected; α_{ST} is the failure probability if one transistor of the ST circuit is affected; $A_R = N_{ST}/N_S$ is a coefficient of hardware redundancy of the ST circuit concerning the synchronous one.

Let us consider that, in combinational circuits, in the worst case, the ratio of complexities of a ST and synchronous circuit equals $A_{R\_C} = 2.7$ (from the practice of various combinational ST circuit types implementation), and the failure probabilities for them are $\alpha_{S1} = 0.5$ and $\alpha_{ST1} = 0.156$ [9]. Such a low failure probability in the ST circuit is due to the completeness of the dual-rail coding of information signals proposed in [6], considering the state opposite to the spacer as a spacer but not forbidden. Then for combinational synchronous and ST circuits:

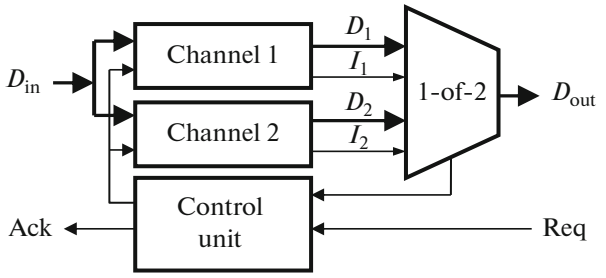

Fig. 1. Soft-error-tolerant ST circuit.

$$K_{I\_C} = \frac{\alpha_{S1}}{A_{R\_C}\alpha_{ST1}} = \frac{0.5}{2.7\times 0.156} = 1.19. \quad (2)$$

For sequential circuits, in the worst case, the ratio of the ST and synchronous counterpart complexities equals $A_{R\_S} = 1.5$, as a comparison of their circuit implementations shows, and their failure probabilities equal $\alpha_{S2} = 0.5$ and $\alpha_{ST2} = 0.17$ [10]. Then:

$$K_{I\_S} = \frac{\alpha_{S2}}{A_{R\_S}\alpha_{ST2}} = \frac{0.5}{1.5\times 0.17} = 1.96. \quad (3)$$

Formulas (1)–(3) demonstrate the best failure tolerance of ST circuits in comparison with synchronous counterparts, despite their hardware redundancy.

4. COMPARISON OF FAILURE-TOLERANT CIRCUITS

Let us estimate the failure-free operation time for tripled synchronous and duplicated ST circuits. In the synchronous circuit, the result is correct if it matches at least two of the three blocks. The failure-free operation probability $R_{M\text{-of-}N}(t)$ for N identical blocks as long as at least M of them work without failure is described by the equation [3]:

$$R_{M\text{-of-}N}(t) = \sum_{i=0}^{N-M}\left\{\frac{N!}{i!(N-i)!}\left[1-R(t)\right]^i R(t)^{N-i}\right\},$$

where $R(t)$ is the failure-free operation probability of one block.

Then, in the synchronous circuit case with majority control ($N = 3$, $M = 2$), the failure-free operation time $T_{FF\text{-}T}$ equals [3]:

$$T_{FF\_T} = \int_0^\infty R_{2\text{-of-}3}(t)\,dt$$

$$= \int_0^\infty \left[3R(t)^2 - 2R(t)^3\right]dt = \frac{5}{6\lambda_S}.$$

In the duplicated ST circuit, $N = 2$, $M = 1$. Then its failure-free operation time:

$$T_{FF\_D} = \int_0^\infty R_{1\text{-}of\text{-}2}(t)\,dt$$

$$= \int_0^\infty \left[2R(t) - R(t)^2\right] dt = \frac{3}{2\lambda_{ST}}.$$

Considering formulas (1)–(3), the ratio of the failure-free operation time of the duplicated ST circuit and the majority case of its synchronous counterpart equals:

$$K_T = \frac{T_{FF\_D}}{T_{FF\_T}} = 1.8\frac{\lambda_S}{\lambda_{ST}},$$

or $K_{T\_C} = 2.14$ for combinational circuits and $K_{T\_S} = 3.53$ for sequential circuits.

Thus, due to their inherent masking of single soft errors, the duplication case of ST circuits has a failure-free operation time 2.1 through 3.5 times longer than their synchronous counterparts with triple modular redundancy. At the same time, their redundancy concerning the synchronous counterparts decreases by 1.5 times. Therefore, they are a promising alternative to synchronous circuits for designing highly reliable microelectronic devices.

The above failure probability estimates α_S and α_{ST} were obtained heuristically, assuming all branches in the "tree" of events generated by a soft error cause have an equal observation probability. One can improve the accuracy of estimates only by using software tools simulating the failure mechanisms in microelectronic components.

CONCLUSIONS

1. Synchronous circuits with N-of-M voting do not protect against highly intensive single and multiple soft errors.

2. In the first approximation, the duplicated ST circuit has 2.1–3.5 times better soft error tolerance than a synchronous counterpart with triple modular redundancy.

3. The new software tools development for simulating the failure mechanisms in microelectronic components will allow to obtain more accurate estimates of the soft error tolerance of electronic circuits and develop more effective failure-tolerant solutions.

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CONFLICT OF INTEREST

The authors declare that they have no conflicts of interest.

REFERENCES

1. Viktorova, V.S., Lubkov, N.V., and Stepanyants, A.S., *Analiz nadezhnosti otkazoustoichivykh upravlyayushchikh vychislitel'nykh sistem* (Reliability Analysis of Fault-Tolerant Control Computing Systems), Moscow: Inst. Probl. Upravl. RAN, 2016. https://www.ipu.ru/sites/default/files/card_file/VLS.pdf. Accessed June 6, 2022.

2. Alagoz, B.B., Boolean logic with fault tolerant coding, *OncuBilim Algorithm Syst. Labs,* 2009, vol. 9, p. 03.

3. Dubrova, E., *Fault-Tolerant Design,* New York: Springer, 2013. https://doi.org/10.1007/978-1-4614-2113-9

4. Zakharov, V., Stepchenkov, Y., Diachenko, Y., and Rogdestvenski, Y., Self-timed circuitry retrospective, in *Proceedings of the International Conference Engineering Technologies and Computer Science EnT 2020, Moscow, Russia, 2020,* pp. 58–64. https://doi.org/10.1109/EnT48576.2020.00018

5. Stepchenkov, Y.A., Kamenskih, A.N., Diachenko, Y.G., Rogdestvenski, Y.V., and Diachenko, D.Y., Fault-tolerance of self-timed circuits, in *Proceedings of the 10th International Conference on Dependable Systems, Services, and Technologies (DESSERT), 2019, Leeds, United Kingdom,* pp. 41–44. https://doi.org/10.1109/DESSERT.2019.8770047

6. Stepchenkov, Y.A., Kamenskih, A.N., Diachenko, Y.G., Rogdestvenski, Y.V., and Diachenko, D.Y., Improvement of the natural self-timed circuit tolerance to short-term soft errors, *Adv. Sci. Technol. Eng. Syst. J.,* 2020, vol. 5, no. 2, pp. 44–56. https://doi.org/10.25046/aj050206

7. Zatsarinny, A.A., Stepchenkov, Yu.A., Diachenko, Yu.G., and Rogdestvenski, Yu.V., Self-timed circuits as a basis for designing highly reliable high-performance computers of the next generation, in *Mathematical Modeling in Materials Science of Electronic Components MMMEK-2020,* Moscow: MAKS Press, 2020, pp. 114–116. https://doi.org/10.29003/m1535.MMMSEC-2020/114-116

8. Monnet, Y., Renaudin, M., and Leveugle, R., Hardening techniques against transient faults for asynchronous circuits, in *Proceedings of the 11th IEEE International Conference: On-Line Testing Symposium, 2005.* https://doi.org/10.1109 /IOLTS.2005.30

9. Stepchenkov, Yu.A., Diachenko, Yu.G., Rogdestvenski, Yu.V., Morozov, N.V., Stepchenkov, D.Yu., and Diachenko, D.Yu., Self-timed pipeline tolerance to soft errors in its combinational part, *Sist. Sredstva Inform.,* 2020, vol. 30, no. 3, pp. 49–55. http://selftiming.ru/new/2020/12/07/ustojchivost-samosinhronnogo-konvejera-k-logicheskim-sboyam-v-kombinaczionnoj-chasti (Accessed June 6, 2022). https://doi.org/10.14357/08696527200305

10. Sokolov, I.A., Stepchenkov, Yu.A., Dyachenko, Yu.G., and Rogdestvenski, Yu.V., Improvement of self-timed circuit soft error tolerance, *Inform. Prilozh.,* 2020, vol. 14, no. 4, pp. 63–68. http://selftiming.ru/new/2021/02/01/povyshenie-sboeustojchivosti-samosinhronnyh-shem (Accessed June 6, 2022). https://doi.org/10.14357/19922264200409